

Claims

1. A method for the fast, timing recovery of transmitted data between two ADSL modems, said data is transferred along a noisy, high loss, high distortion ^{transmission medium} wiring, characterized by that data received at the slave modem as a sequence of symbols, is sampled at the symbol rate, converted to digital form, said sampled data been split to In-phase (I) and Quadrature (Q) channels, filtered with a digital Low-Pass Filter (LPF), sampled again at twice the symbol rate, and modulated each with the two discrete-time

sequences $\cos(0.5\pi n) = \dots, 1, 0, -1, 0, \dots$
 $\sin(0.5\pi n) = \dots, 0, 1, 0, -1, \dots$

2. A method according to claim 1, comprising the steps of:

- a) Providing a master ADSL modem, synchronized by its own timing clock, for data transmission to a second slave ADSL modem;
- b) Providing a second slave ADSL modem, synchronized by its own timing clock, for data reception from said master ADSL modem;
- c) Providing a communication wiring connecting said master modem to said slave modem;
- d) Encoding and transmitting the desired data as a sequence of symbols to the slave modem using pre-determined QAM states;
- e) Receiving the transmitted symbols at the slave receiver (demodulator);
- f) Sampling the received signal;
- g) Splitting the sampled data to in-phase (I) and quadrature (Q) channels;
- h) Filtering each channels of step g) above with digital low-pass filters, said filters

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being matched to the transmitting filters at the master modem;

i) Turning the master clock timing recovery into blind mode, by the steps of:

(1) Sampling the filtered I and Q outputs at twice the symbol rate;

(2) Extracting the lower and upper band edge components by modulating each of the sampled sequence of I and Q outputs of step (1) above with two discrete time

sequences: $\cos(0.5\pi n) = \dots, 1, 0, -1, 0, \dots$;
 $\sin(0.5\pi n) = \dots, 0, 1, 0, -1, \dots$;

(3) Filtering the four resulting products with four first order low-pass filters and re-sampling the results at the symbol rate;

(4) Computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Filtering both the real and the imaginary parts of step (4) above, using another first order low-pass filter;

(6) Normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC);

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- (10) Using a secondary accumulator to correct the control word supplied to the DAC of step (9) above;
- j) Feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;
- k) Computing the symbol state data decisions using a slicer circuitry;
- l) Fine equalization of the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which are extracted from the slicer I and Q inputs, respectively;
- m) Computing the extracted symbols error rate at the slicer outputs; and
- n) After the error probability decreases to a given BER, switching from blind mode timing recovery to data directed timing recovery mode.

a 3. A method according to claims ~~1 and 2~~, wherein the transmission medium is a pair of copper wires.

a 4. A method according to ~~any one of claims 1 to 3~~, wherein the pair of copper wires is a telephone line.

a 5. A method according to claims ~~1 and 2~~ wherein the sampling rate is more than twice the symbol rate.

a 6. A method according to claims ~~1 and 2~~, wherein the timing oscillator utilized by the phase-locked loop is a Voltage-Controlled Crystal Oscillator (VCXO) or the like suitable clock oscillator.

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7. A method according to ~~any one of claims 1 to 6~~, wherein the blind timing recovery is achieved using a reduced constellation.

8. A method according to claim 7, wherein the reduced constellation comprises only equal amplitude symbols.

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9. A method according to claim ~~1 to 6~~, wherein the blind timing recovery is achieved using full constellation.

10. A method according to claim ~~1 and 2~~, wherein the control signal of the PLL tracking oscillator is provided accurately and converted using an up to 8 bit Digital to Analog Converter (DAC) means, comprising the steps of:

- a) Rounding the double precision control signal;
- b) Generating an error signal between the double precision value and the rounded value;
- c) Accumulating the error signal in a secondary accumulator;
- d) Adding the error signal to the output signal of the secondary accumulator;
- e) Comparing the result of step d) above with half the value of the DAC's LSB;
- f) Compensating the rounded value according to the result of step e) above by the steps of:
 - (1) Adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; or

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(2) Subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB.

11. A method according to any one of claims 1 to 10, substantially as described and illustrated.

12. An XDSL modem for fast timing recovery of received data, said data transmitted between two XDSL modems and transferred through a noisy, high loss, high distortion wiring, comprising:

- a) Circuitry for receiving the transmitted symbols at the slave receiver (demodulator);
- b) Circuitry for sampling the received signal;
- c) Circuitry for splitting the sampled data to in-phase (I) and quadrature (Q) channels;
- d) Circuitry for filtering each channels of step c) above with digital low-pass filters, said filters being matched to the transmitting filters at the master modem;
- e) Circuitry for turning the master clock timing recovery into blind mode, by the steps of:

- (1) Circuitry for sampling the filtered I and Q outputs at twice the symbol rate;
- (2) Circuitry for extracting the lower and upper band edge components by modulating each of the sampled sequence of I and Q outputs of step (1) above

with two discrete time sequences:

$$\cos(0.5\pi n) = \dots, 1, 0, -1, 0, \dots$$

$$\sin(0.5\pi n) = \dots, 0, 1, 0, -1, \dots$$

- (3) Circuitry for filtering the four resulting products with four first order low-

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pass filters and re-sampling the results at the symbol rate;

(4) Circuitry for computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Circuitry for filtering both the real and the imaginary parts of step (4) above, using one or more first order low-pass filter;

(6) Circuitry for normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Circuitry for extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Circuitry for feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Circuitry for converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC);

f) Circuitry for feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;

g) Circuitry for computing the symbol state data decisions using a slicer circuitry;

h) Fine equalizing the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which is extracted from the slicer I and Q inputs, respectively;

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- i) Circuitry for computing the extracted symbols error rate at the slicer outputs; and
- j) Circuitry for switching from blind mode timing recovery to data directed timing recovery mode, once the error is reduced to less than a given BER.

a 13. A modem according to claim 12, further comprising ~~(10)~~ circuitry for accumulation to correct the control word supplied to the DAC by providing:

- a) Circuitry for rounding the double precision control signal;
- b) Circuitry for generation of an error signal between the double precision value and the rounded value;
- c) Circuitry for accumulation of the error signal in a secondary accumulator;
- d) Circuitry for adding the error signal to the output signal of the secondary accumulator;
- e) Circuitry for comparing the result of step (d) above with half the value of the DAC's LSB;
- f) Circuitry for compensating the rounded value according to the result of step (e) above and by:

- (1) Circuitry for adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; and
- (2) Circuitry for subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB.

14. A modem according to claim 12, comprising means for sampling at a sampling rate that is more than twice the symbol rate.

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